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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,754	03/08/2004	Sun-Ha Hwang	4591-393	4368

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EXAMINER

KIM, SU C

ART UNIT PAPER NUMBER

2823

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

4 EJC

Office Action Summary	Application No. 10/796,754	Applicant(s) HWANG ET AL.	
	Examiner Su C. Kim	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-17 is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/8/04</u> | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "13A"(page 1 line 22), "13B"(page1 line 24), "18B"(page 1 line 32), " 108" (page 7, line 16) and "112" (page 8, line 10). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

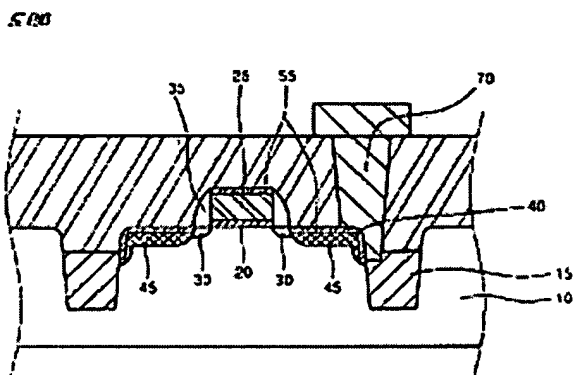
A person shall be entitled to a patent unless –

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(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 are rejected under 35 U.S.C. 102(a) as being anticipated by **Baek** (Kr 1020010065747).



Baek discloses a semiconductor process as claimed. **See all FIGS** where Baek teaches the following limitations

4. With respect to claim 1, Baek discloses a method of fabricating a semiconductor substrate, comprising:

forming an isolation layer **15** in a substrate **10** of first conductivity type, the isolation layer formed with an outline to define an active region (please note that active region is between isolation regions);

diffusing impurities of second conductivity type in a predetermined region of the active region to form an impurity diffused region;

recessing a region of the device isolation layer **15** and exposing a portion of the first conductivity type material under the impurity diffused region; and

forming a salicide layer **55** covering the impurity diffused region and covering the portion **40** of the first conductivity type material exposed by the recess.

2. With respect to claim 2, Baek discloses the recess **15** is formed by etching to a depth deeper than a depth of the impurity diffused region.

3. The method of claim 1, in which the forming the salicide layer **55** comprises:

forming metal **55** on exposed surfaces of the resultant structure including the active region (please note that it is well known active region is between the isolation regions on a semiconductor substrate) and walls of the recess **40** (please note the edge of element 40) ; and

annealing the metal layer **70** to diffuse atoms of the metal into portions of the active region in contact with the metal and into portions the substrate of first conductivity type in contact with the metal, and siliciding **55** (please note that it is well known to interpret "salicide" as self-aligned silicide) the surface of the active region as well as a surface of the substrate of first conductivity type exposed by the recess.

5. Claims 5-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Violette et al. (US 5741735).

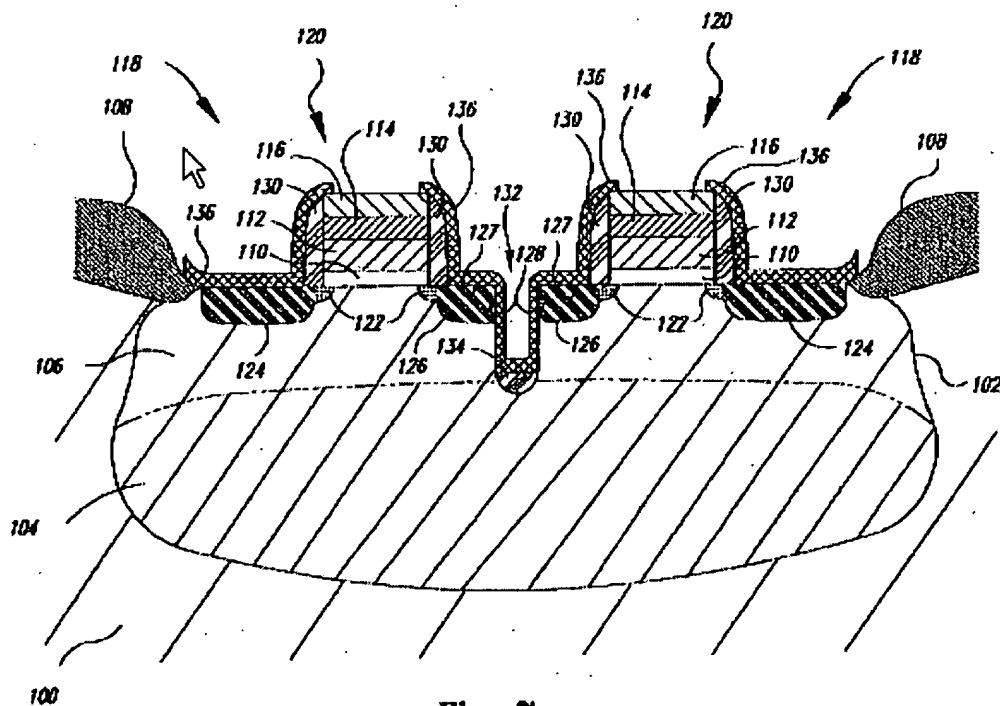


Fig. 7

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Violette disclose a semiconductor process as claimed. See FIG. 1-10 where Violette teaches the following

6. With respect to claim 5, Violette discloses that a method of fabricating a semiconductor device, comprising:

forming a device isolation layer **108** in a predetermined region of a substrate **100** of first conductivity type (doped P-type, column 3, line 10) to define an outline to an active region;

forming a gate pattern **120** crossing the active region;

forming a source/drain region **124 & 122** of second conductivity type in the active region (N-type, column 3, line 55) at both sides of the gate pattern;

patterning the device isolation layer (please note that it is well known to pattern the isolation region on a semiconductor substrate) and forming a recess that exposes a portion of the substrate of first conductivity type (please note that Applicant's claim language does not require the isolation regions to contain the recess), the portion exposed adjacent to the source/drain region of second conductivity type at one side of the gate pattern; and

siliciding **136** a surface of the source/drain region of second conductivity type and a surface of the substrate of first conductivity type exposed by the recess.

7. With respect claim 6, Violette discloses the method of claim 5, in which the forming the recess comprises etching the device isolation layer **108** to a depth deeper than the thickness of the source/drain region of second conductivity type.

8. With respect to claim 7, Violette disclose the method of claim 5, in which the forming the gate pattern comprises:

forming a gate insulation layer **110** over the active and

a gate conductive layer **112** over the gate insulation layer;

patterning the gate conductive layer **120** and

forming a gate electrode **112** crossing the active region;

and forming a sidewall spacer **130** against a sidewall of the gate electrode.

9. With respect to claim 8, Violette discloses the method of claim 7, in which the forming the source/drain region of second conductivity type comprises:

after forming the gate electrode, implanting impurity ions into a first surface region of the active region **124**, using the gate electrode as an ion implantation mask during the implanting, and forming a lightly diffused layer **122** into the first surface region at both sides of the gate electrode;

and after forming the sidewall spacer **130**, implanting impurity ions **124 & 122** into a second surface region of the active region, using the gate electrode **112** and the sidewall spacer collectively as an ion implantation mask during the implanting into the second surface region, and forming a heavily diffused layer **124** into the second surface region at both sides of the gate electrode with sidewall spacer;

the heavily diffused layer **124** formed with a depth deeper than the depth of the lightly diffused layer **122**.

10. With respect to claim 9, Violette disclosed the method of claim 5, in which the siliciding comprises:

forming metal **136** on the exposed surface of the source/drain region and on the portion of the substrate of first conductivity type exposed by the recess;

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and annealing the metal 136 on the exposed surfaces to silicide a surface of the source/drain region of second conductivity type in contact with the metal and to silicide a surface of the substrate of first conductivity type in contact with the metal and facing the recess (column 4 lines 14-21).

11. With respect to claim10, Violette discloses the method of claim9, in which the siliciding 136 further comprises siliciding a top surface of the gate electrode to form a gate silicide layer 136.

12. With respect to claim11, Violette disclosed the method as claimed in claim9, in which the metal comprises at least one of cobalt, nickel, and titanium (column 4, lines 19-20).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baek in view of Violette.

15. With respect claim 4, Baek fails to teach the method of claim3, in which the metal comprises at least one material selected from the group consisting of cobalt, titanium, and nickel.

Violette teaches at least one material selected from the group consisting of cobalt, titanium and nickel.

In view of Violette, it would have been obvious to one of ordinary skill in the art to incorporate the material of Violette into the Baek semiconductor process because titanium can be a self-aligned silicide (salicide)(column 4, line 20-21)

Allowable Subject Matter

16. Claims 12-17 are allowed.

Reason for Allowance

17. The prior art does not anticipate nor render obviousness as to a method of forming a salicide by forming a recess.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday through Friday, 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, CHAUDHURI OLIK can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. DAVID COLEMAN
PRIMARY EXAMINER